Explorations on Open-Source FPGA Development with Wireless Audio System

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Background

Field Programmable Gate Arrays (FPGAs) are specialized electrical components that can be customized for many different computational applications to get the performance of an ASIC along with the versatility of an MCU. FPGAs can be used for edge computing to provide flexible fast computation associated with control, RF, and machine learning applications.

Audio processing is a topic newly becoming popular in the area of FPGA starting with different smart speakers gaining popularity. However, audio processing is just another form of signal processing which is a traditional type of FPGA functionality in many systems.

With the cost of FPGA chips dramatically decreases in recent years, many open source projects targeting FPGAs have emerged.

Objectives

Build a wireless audio system utilizing FPGA's capabilities to evaluate current open source FPGA development effort.

The detailed goals/objectives of this project were:

- To develop a useful, low cost, solution for FPGA assisted wireless audio system
- To support multiple microphones
- To support arbitrary near real-time filters on cost-effective performance-limited platforms
- To extend an audio interface for low-end MCUs that does not have I2S input or output.
- Evaluate current open source FPGA development efforts for further projects need in our research group

References

[1] Enjoy-Digital, "enjoy-digital/litex," GitHub, 16-May-2019. [Online]. Available: https://github.com/enjoy-digital/litex. [Accessed: 16-May-2019].
[2] B. Kipnis, "FirGen/MultGen :: OverviewOverviewNewsDownloadsBugtracker," OpenCores, 20-Dec-9AD. [Online]. Available: https://opencores.org/projects/fir_filter_generator. [Accessed: 16-May-2019].

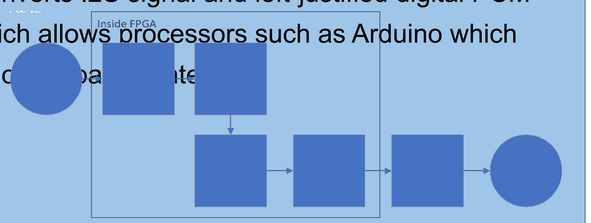
Process & Solution

The system is divided into 2 parts: processor and FPGA. The FPGA as indicated in the objective section, will handle: PDM microphone input and aggregation, audio interface extension for processor, necessary audio filtering for audio quality.

The processor we have chosen is ESP32 as it supports an open-source SDK named "ESP-ADF" which enables us to do easy and powerful development for an audio system based on the platform. The system will function as a Wi-Fi enabled audio broadcast, allowing its client to receive real-time stream from the microphone array.

Implantations of PDM and audio interface extension are straight forward. We referenced open-source I2S IP cores and ported it to our design. Our design converts I2S signal and left-justified digital PCM audio through SPI which allows processors such as Arduino which doesn't have any audio capabilities.

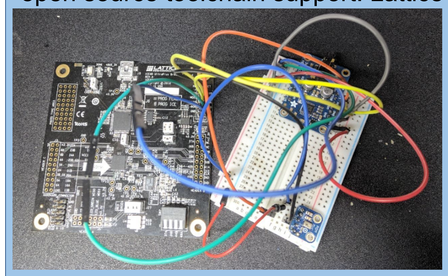
The harder part is the implementation of the filter part. Our team members don't have practical experiences in digital filter designs, even if some members have studied filters in class settings. After doing some research, we found out the proprietary IP core on FIR filters are much more mature compare to open-source IP cores: Most of the open-source filter IP cores are either unfinished or only applicable in a very narrow range of specific applications. The only partially useable finished FIR filter is written in VHDL and we can only understand it to implement it partially in our project. We end up deciding to implement EQ using FFT IP cores which is easier to find and understand.



System Component Diagram

We did and have proposed to use other more integrated and mature open-source solutions to solve this project challenge. One of the most promising framework we have looked at is LiteX. LiteX is a mature and general FPGA framework built on a high-level hardware design language named Migen. It even has its own DDR and PCIe controller implemented and open-sourced. However, LiteX needs specific platforms to be deployable, and most of those platforms are either old or expensive. Cost-effective FPGAs developed in recent years by market new-comers are not supported yet, despite FPGA open-source tooling community worked hard on them and provides brilliant support on these chips.

The Lattice iCE40 is an FPGA chip suitable for this design. Its DSP core will improve the latency of filter algorithm and enable fast overall functionality using minimum power and area. Its official support of neural network will make further development of noise canceling and receiver beam-forming easily accomplishable. It's also cost effective which makes the cost significantly lower compare to any other FPGA solution that accomplish the same goal easily. iCE40 has another noticeable feature: its free and open source toolchain support. Lattice open source tools provides official free toolchain to develop on this FPGA, and it's also the only FPGA that can be implemented in a design with only open-source code and components.


FPGA Design Prototype

Conclusions

- Open-source FPGA IP cores are not mature enough compare to the open-source tooling. We faced a lot of unnecessary trade-offs compare to using proprietary / vendor-provided IPs and tools.
- The current stage of development of open FPGA works mainly focused on control and connectivity, and complex computing / algorithmic IP cores are still mainly only available from commercial vendors.
- Open source technologies can help to create cutting-edge solutions while keeping it cost-effective.

Acknowledgements

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